

General Description

The NCR 53C400 SCSI host adapter chip is a 68-pin CMOS integrated circuit designed to interface the Small Computer Systems Interface (SCSI) bus to an IBM PC, XT, AT or PS/2 model 25, 30 or 30-286 I/O channel bus or compatible. This high performance host adapter circuit retains software compatibility with the NCR 5380/C80 SCSI chip while providing improved asynchronous SCSI bus performance and data buffering to match speeds between the SCSI bus and the host bus. The 53C400 also provides special high-current output drivers capable of sinking 48 mA at 0.5 V, thereby allowing for direct connection to the SCSI bus. This chip can significantly reduce the part count of a SCSI host adapter.

The 53C400 provides an eight-bit interface to the family of IBM PCs and compatibles. It communicates with the host microprocessor as a memory-mapped device. Base memory address is switch selectable between eight choices. The interrupt level of the chip can be programmed for interrupt sharing as required by the PS/2 systems.

Data transfer is accomplished via Programmed Input/Output (PIO) operation and DMA is thus not required. Speed matching is accomplished by the 53C400 with the use of two 128-byte independent data buffers that can burst data up to the I/O channel's limit. To facilitate the implementation of an external BIOS ROM, a 64-byte scratchpad RAM is included on the chip.

The 53C400 is available in a 68-pin Plastic Leaded Chip Carrier (PLCC) package.

SCSI Interface Features

- ANSI X3131-1986 compatible
- On-chip 48 mA drivers
- Up to 2.0 MB/S asynchronous SCSI
- Initiator or target roles
- Parity generation, optional checking
- Direct control of SCSI bus signals
- Basic Winchester disk BIOS available

PC (I/O Channel) Interface Features

- Memory-mapped PC interface
- Interrupt/non-interrupt operation
- Switch selectable base memory address
- Programmable interrupt level
- 8-bit data interface
- Two internal 128-byte rotating buffers
- Internal 64-byte scratchpad RAM
- 1.2 MB/S burst transfer rate (6 MHz PC/AT at zero-wait state)