

General Description

The 53C90A and 53C90B are high performance CMOS devices conforming to the ANSI standard, X3.131-1986, for Small Computer Systems Interface (SCSI). They are a super-set of the 53C90 with additional commands and a second configuration register. The C90A is intended to directly replace a C90 in an existing design, allowing an easy upgrade to SCSI-2. The C90B has a parity pin on the host processor interface, but is otherwise identical to the C90A. Both are 100% compatible with existing 53C90 software.

The C90 family reduces protocol overhead by performing common SCSI algorithms, or sequences, in response to a single C90 command. The C90A and C90B will operate at sustained data transfer rates of 5 MB/S in synchronous mode and 5 MB/S in asynchronous mode. Refer to *Data Transfer Rate*.

Features

- ANSI X3.131-1986 compatible
- On-chip 48 mA drivers
- Control logic for differential transceivers
- Parity generation, optional checking
- Parity pass through (53C90B only)
- Programmable transfer period
- Programmable offset
- SCSI-2 tagged-queuing
- 16-byte FIFO
- 12 MB/S DMA interface
- Up to 5 MB/S asynchronous SCSI
- Up to 5 MB/S synchronous SCSI
- 25 MHz clock
- Low power CMOS
- 68-pin PLCC and 80-pin QFP

Figure 1. Functional Block Diagram

